Abstracts

An integrated CMOS distributed amplifier utilizing packaging inductance

P.J. Sullivan, B.A. Xavier and W.H. Ku. "An integrated CMOS distributed amplifier utilizing packaging inductance." 1997 Transactions on Microwave Theory and Techniques 45.10 (Oct. 1997, Part II [T-MTT] (Special Issue on Interconnects and Packaging)): 1969-1976.

An integrated CMOS distributed amplifier is presented. The required inductance needed for the distributed waveguide structure is realized by the parasitic packaging inductance of a plastic surface-mount package. A fully packaged three-stage distributed amplifier fabricated in a 0.8-/spl mu/m CMOS process is presented. The distributed amplifier has a unity gain cutoff frequency of 4.7 GHz, a gain of 5 dB, with a gain flatness of /spl plusmn/1.2 dB over the 300-kHz to 3-GHz band. At a frequency of 2 GHz the amplifier has an input referred third-order intercept point of +15 dBm and an input referred 1-dB compression point of +7 dBm. The amplifier consumes 18 mA from a 3.0-V supply. The distributed amplifier is matched to 50 /spl Omega/ at the input and output and has a maximum input voltage standing-wave ratio (VSWR) of 1.7:1, and a maximum output VSWR of 1.3:1 over the 300 kHz to 3 GHz band. The amplifier has a noise figure of 5.1 dB at 2 GHz.

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